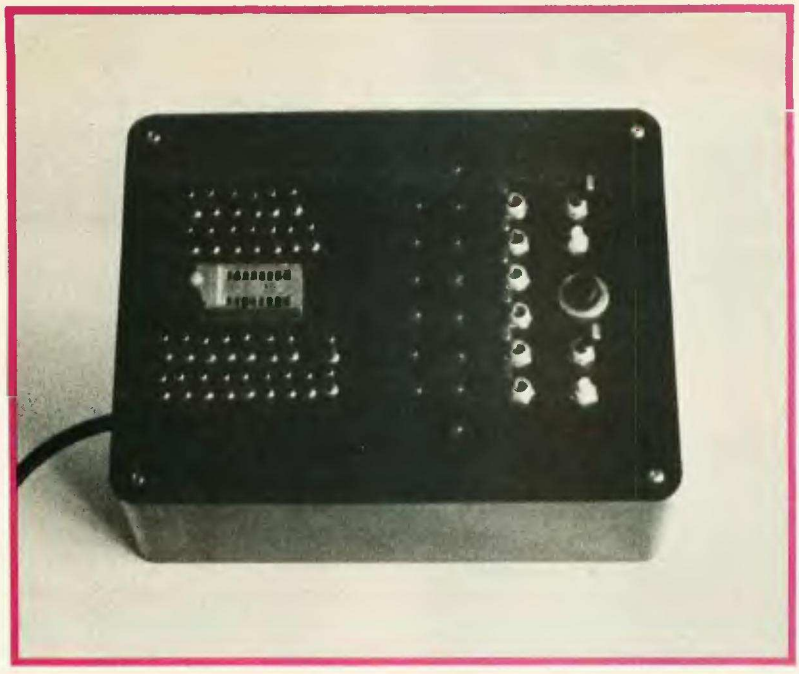

Photo 1: The prototype for the author's IC tester. The LEDs shown were not included in the final design of figure 1.

A Programmable IC Tester

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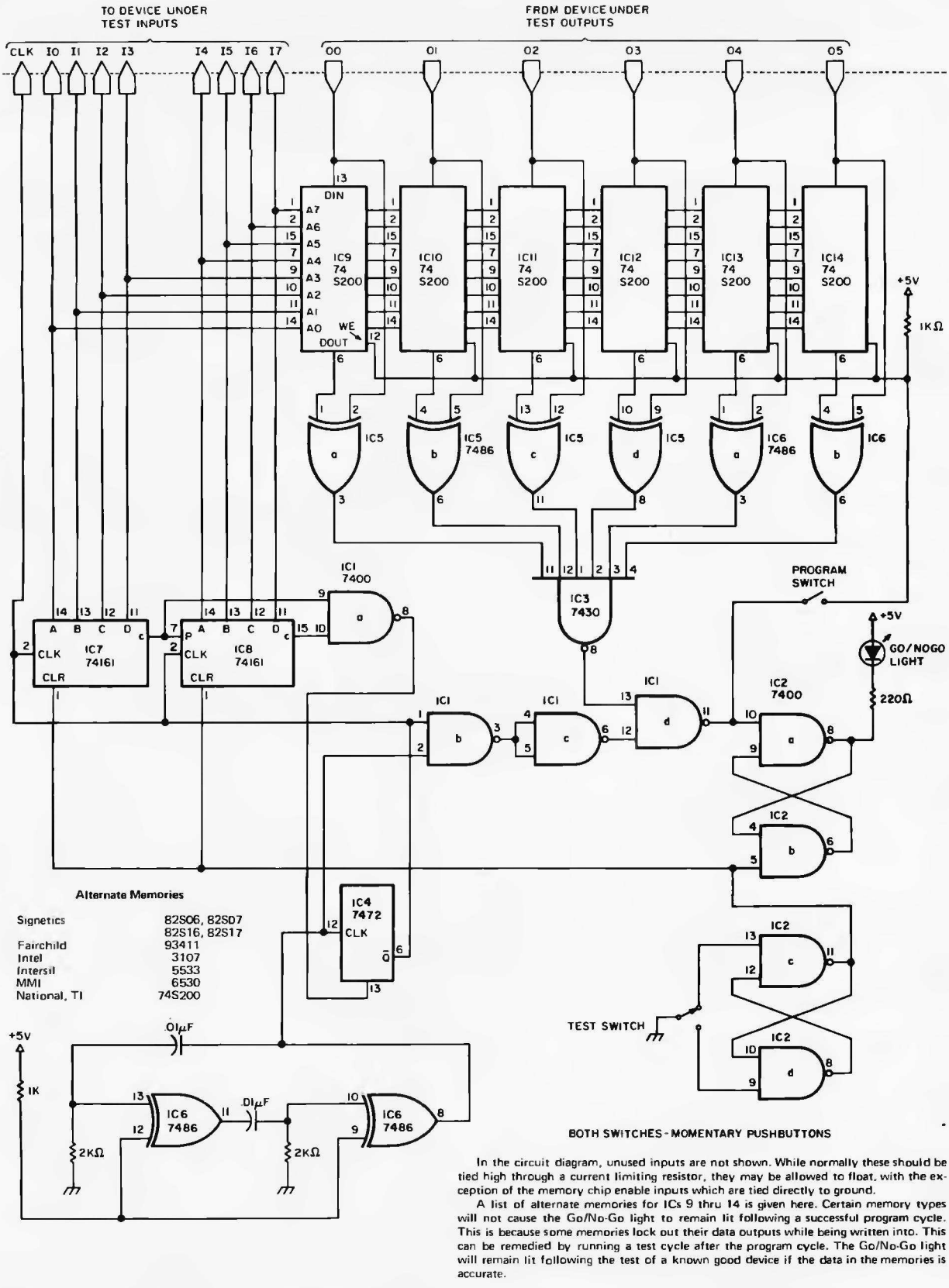
The high cost of digital components can be significantly reduced by the construction of this simple test instrument. While components of questionable reliability have long been available for a fraction of their value, the experimenter has been unable to take full advantage of them for lack of an adequate means of component testing. This circuit, however, now offers such a means for the rapid and accurate screening of bargain components.

Conventional component testing generally takes the form of either building a prototype circuit and substituting devices until it works, or setting up a rig of lights and switches and testing each gate or flip flop on the chip individually. Although these procedures are sufficient for the construction of trivial circuits employing a small number of integrated circuits, neither is exacting enough nor fast enough to provide the quantity or quality of parts required for a well stocked electronics lab. The main weakness of both approaches is their failure to check the devices in question under *all* possible conditions of data. As an example, consider the 7400 quad NAND gate with the failure condition of an internal short between the input on pin 4 and the output on pin 3. If this device is either tested in a circuit employing the quad NAND gate without using the input on pin 4, or tested in a rig in which each gate is tested individually, then the device will be passed without the failure conditions ever having been met. To be certain of testing all possible failure modes of this device, all 256 possible data conditions on the eight device inputs must be checked, a prohibitive requirement for manual testing.

To this end, the circuit shown in figure 1 has been designed to provide an automatic, instantaneous and exhaustive test of most SSI and MSI components. [SSI (small scale integration) refers to gates, inverters, flip flops, etc, while MSI (medium scale integration) refers to counters, latches, shift registers, etc.] The circuit operates by sending eight lines of input data to the device under test (DUT) and receiving six lines of output. Upon depression of

About the Author

Mark Thorson is currently an undergraduate at the University of California at Berkeley majoring in neurobiology, and has been working with digital logic since sixth grade. (Early efforts involved discrete components and incandescent lamps.)



Alternate Memories

Signetics	82S06, 82S07 82S16, 82S17
Fairchild	93411
Intel	3107
Intersil	5533
MMI	6530
National, TI	74S200

In the circuit diagram, unused inputs are not shown. While normally these should be tied high through a current limiting resistor, they may be allowed to float, with the exception of the memory chip enable inputs which are tied directly to ground.

A list of alternate memories for ICs 9 thru 14 is given here. Certain memory types will not cause the Go/No-Go light to remain lit following a successful program cycle. This is because some memories lock out their data outputs while being written into. This can be remedied by running a test cycle after the program cycle. The Go/No-Go light will remain lit following the test of a known good device if the data in the memories is accurate.

Figure 1: The author's automatic integrated circuit tester. The unit is connected by probes to the inputs of the integrated circuit under test (up to eight inputs can be accommodated). 256 different combinations of logic levels are sent to the integrated circuit, and a running comparison of up to six data outputs from the device is made with a set of results stored in memory for another integrated circuit of the same type that is known to be good. Any deviation from the accepted pattern causes an LED to be lit. The unit is capable of testing both combinatorial ICs, such as logic gates, and sequential ICs, such as flip flops. A learn mode allows the tester to store the characteristics of virtually any TTL integrated circuit in memory for testing.

Number	Type	+5 V Pin	Gnd Pin
IC 1	7400	14	7
IC 2	7400	14	7
IC 3	7430	14	7
IC 4	7472	14	7
IC 5	7486	14	7
IC 6	7486	14	7
IC 7	74161	16	8
IC 8	74161	16	8
IC 9 thru IC 14	74S200 (or equivalent)	16	8

Table 1: Power wiring table for figure 1. See figure 1 for alternate memory ICs for IC9 thru 14.

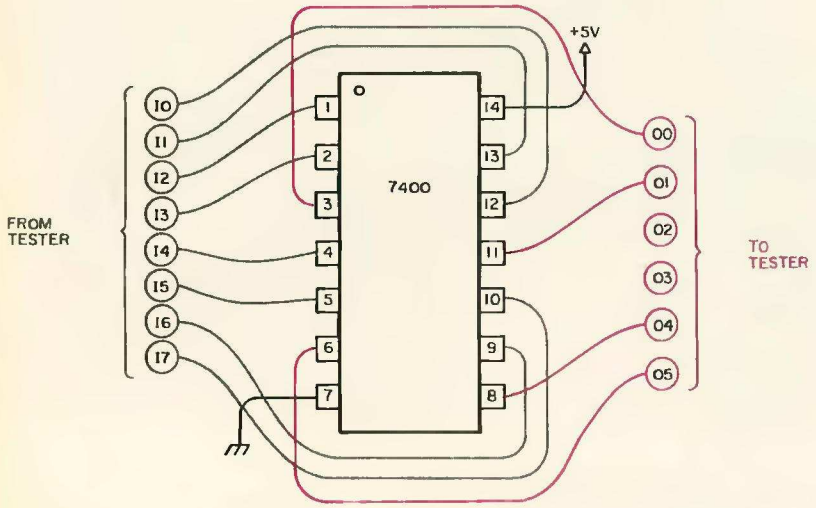


Figure 2: One method of hooking the tester up to a 7400 TTL integrated circuit.

the Test button, the binary counter driving the DUT input lines is cleared and the flip flop driving the Go/No-Go light is set. Upon release, the counter increments through all 256 input conditions to the DUT. Between counts, the data on the six DUT output lines is compared with the data stored in memory, and if any mismatch occurs, the Go/No-Go flip flop is cleared. Once the counter reaches its terminal count, the clear input to the clock oscillator flip flop is driven low, thereby inhibiting further counts until the Test button is hit again. At this time, if the Go/No-Go light has remained lit, the component has passed the test. Programming is accomplished by holding the Program button down during a test cycle of a known good device. During this time, data on the DUT outputs is loaded into memory between counts on the DUT input lines. Once the PROGRAM button is released, data in the memory is protected by a pull-up resistor on its read/write line.

Combinatorial integrated circuits, that is, integrated circuits such as gates or comparators which do not contain storage elements such as flip flops, are tested by connecting all device inputs to lines I_0 to I_7 and all device outputs to lines O_0 to O_5. Any ordering of the connections is satisfactory, because the tester will run through all possible input conditions despite the arrangement used. Sequential integrated circuits, however, require special consideration due to their internal data states. A device such as the 74161 4 bit binary counter, for example, will require its clock input to change at least 32 times faster than its clear input to insure the completion of a full counting cycle before being cleared. To aid in the testing of sequential integrated circuits with several clear, preset, inhibit, and other combinatorial inputs, the clock input has been provided which toggles twice as fast as I_0. This input is useful for connecting to the clock input of counters, flip flops, and shift registers, but should not be used with combinatorial devices or the combinatorial inputs of sequential devices.

As an example of the use of the tester, consider again the 7400 quad NAND gate. This device has a total of eight data inputs and four data outputs to be connected. An example of one possible configuration of the connections is shown in figure 2. It should be noted that two DUT outputs are allowed to float. This is permissible, because the same data will be present during a test cycle as when the tester is programmed. It is also acceptable to use less than eight DUT inputs, because the tester will still run through all possible data conditions on the remaining inputs. Once the proper connections have been made, the tester is programmed by inserting a known good device into the DUT socket and holding the Program button down while momentarily depressing the Test button. If the tester has accurately stored the characteristic output of the device, the Go/No-Go light will remain lit following the release of the Test button. The Program button may now be released and tests performed by inserting a questionable device and depressing the Test button. If the Go/No-Go light remains lit upon release of the Test button, the device has passed.

As an example of the testing of a sequential device, consider the 74161 4 bit binary counter. An example of one possible configuration of its connections is shown in figure 3. Unlike the case of the quad NAND gate, the ordering of the DUT input connections is very important. Combinatorial inputs such as clear, load, and inhibit are

put on the more slowly toggling lines I_4 to I_7, and the sequential inputs are put on the faster lines I_0 to I_3. This example also illustrates the use of the clock line for the clock. It should be noted that there is a minimum separation of four lines between the clock and any combinatorial input. As previously stated, this is necessary to allow the counter to complete a full counting cycle. Strictly speaking, the presetting inputs to the counter are also combinatorial inputs, but they do not interfere with the counting cycle, so they may be placed within four lines of the clock. They are, however, synchronous inputs and as such may not be placed on a DUT input line which toggles faster than the clock. Also, while the ordering of the DUT inputs is important (for reasons just explained), there are no restrictions whatsoever on the ordering of the DUT output connections. Connections between the integrated circuit tester and the DUT socket should be made via banana plugs, matrix switches, or other forms of connection which readily permit modification. The DUT socket itself should be a zero insertion force (ZIF) type socket (Textool or equivalent).

Expansion of the testing capacity of the unit can be achieved by extending the counter length or the memory size, but it has been my experience that the combination of eight inputs and six outputs has proven ideal for testing most standard TTL components. In my first prototype (see photo 1), a single step feature was provided by switching in a debounced pushbutton switch in place of the oscillator, and placing LED indicator lights on the DUT inputs and on the memory data outputs. This made it possible to examine the memory once it had been programmed and verify that the tester was really doing what it was supposed to do. This feature was also necessary because the original version had to be programmed manually, but the 10 to 15 minutes required to program the tester for even a device as simple as a quad NAND gate made the advantages of autoprogrammability quite apparent. Nevertheless, the single step feature may prove useful to the hobbyist who may wish to use this instrument as a logic analyzer. Other features that may prove useful would be the addition of low power TTL buffers on the DUT outputs to permit testing of CMOS integrated circuits, miniaturized construction for portable operation, and installation of an ammeter in series with the DUT socket power input pin to provide a measure of power dissipation.■

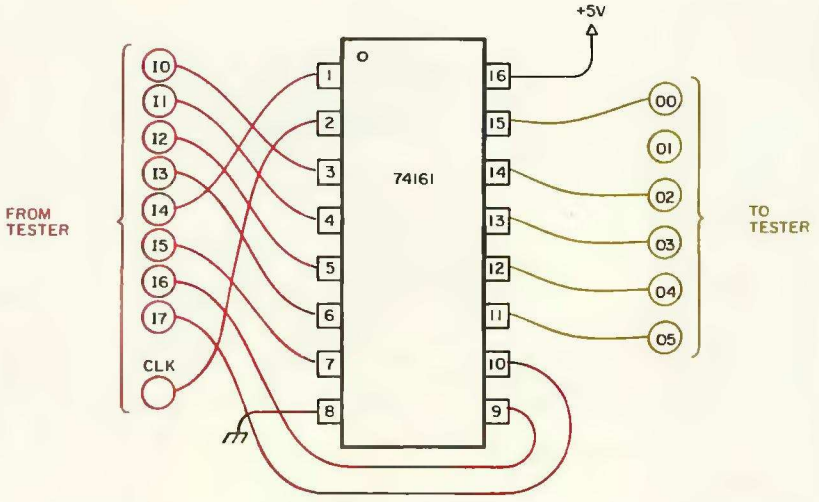


Figure 3: Tester hookup for a TTL 74161 integrated circuit. Note the use of the clock line coming from the tester. This is to ensure that the integrated circuit receives clock signals of the proper speed relative to the other test input lines.