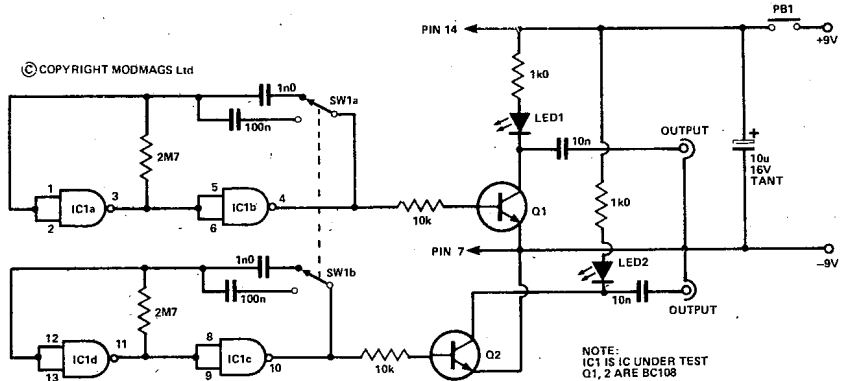


# CMOS tester

C. Jordan, Sompting

This circuit was designed to test 4001 and 4011 devices which were suspected of being damaged due to static from

careless handling. Two gates on each side of the 14 pin DIL package are tested independently. Each pair is connected as an astable, the timing capacitor being switched to allow the device to oscillate at two different frequencies.

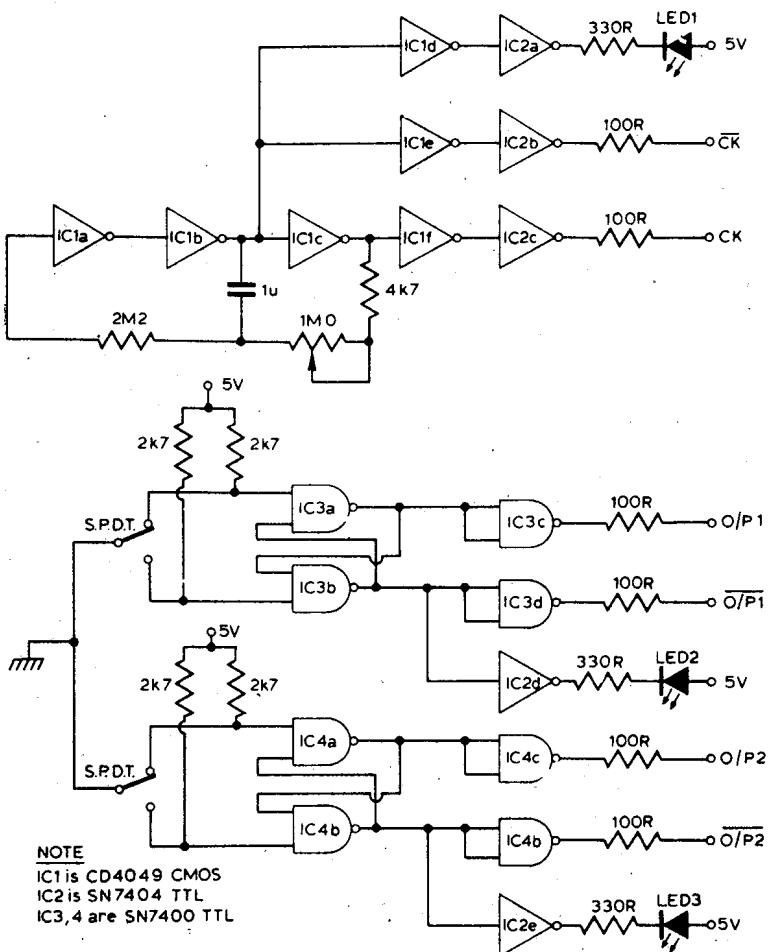


The output of the astable is fed to a transistor which acts as a buffer, driving the LED and providing an audio output to a crystal earpiece. PB1 should be a push-to-make type, so that it is impossible to insert or remove a device with the power on. Although intended to test 4001 and 4011 devices, it will also quite happily test 4030, 4071, 4077, 4081 and 4093.

# Test unit for sequential logic

Any one testing a sequential logic circuit requires input pulses free of contact bounce. This unit does this, providing two switched, jitter-free outputs and a 'slow' variable speed clock. The complements of these signals are also provided.

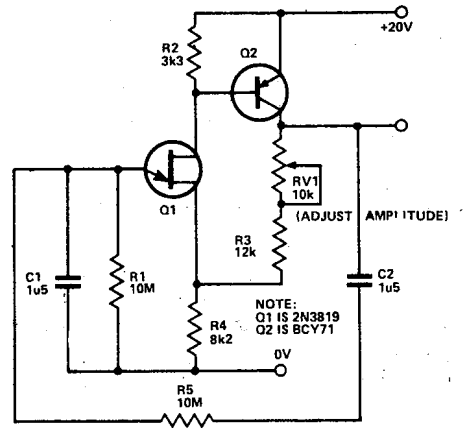
The components shown give the clock a frequency range of 1-200 Hz. The clock's buffered output will drive up to two TTL inputs. The 100R resistors on all outputs provide some measure of accidental short circuit protection.



# VLF sine generator

Generating very low frequency sine waves (i.e. less than 0.1 Hz) presents several problems, Timing capacitors usually have to be large valve electrolytics, any amplifier used must be D.C. coupled, and the amplifier's input impedance must be very high. One standard method is to first generate low frequency square waves, and then to shape these into an approximation of a sine wave by the use of several non linear devices, such as diodes. The circuit shown in Fig. 1 is a relatively simple approach based on the familiar Wien bridge. An n-channel FET and a pnp transistor are arranged in a DC coupled circuit and the voltage gain is determined by the negative feedback R3 and R4. The gain need only be about three, thus if the bias required by the FET is 3V the output level will be approximately half the supply voltage.

Since R1 can be a high value resistor the value of the capacitor is only 1u5 for sine wave outputs of 0.01 Hz. This capacitor is available in polycarbonate. The amplitude of the output can be adjusted by RV1 to give low harmonic distortion and to be about 10V peak to peak. As expected, with this Wien bridge circuit, frequency stability is good with changes in both supply voltage and temperature.



NOTE  
IC1 is CD4049 CMOS  
IC2 is SN7404 TTL  
IC3,4 are SN7400 TTL

NOTE:  
Q1 IS 2N3819  
Q2 IS BCY71